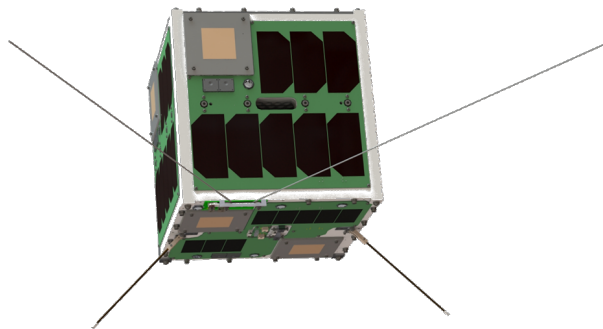


# TUBiX10

## Communication System Specifications



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## Acronyms

**ADCS** Attitude Determination and Control System.

**AIR** Air/Radio Interface.

**ARQ** Automatic Repeat Request.

**COSPAR** Committee on Space Research.

**CRC** Cyclic Redundancy Check.

**EPS** Electric Power System.

**LEOP** Launch and Early Orbit phase.

**LSB** Least Significant Bit.

**LTU** Link Transmission Unit.

**NORAD** North American Aerospace Defense Command.

**OBC** On Board Computer.

**PDU** Payload Data Unit.

**S-Net** S Band Network for Cooperative Nanosatellites.

**SALSAT** Spectrum Analysis Satellite.

**SatNOGS** Satellite Networked Open Ground Station.

**SCN** Satellite Catalog Number.

**SDR** Software-defined radio.

**STNC** S band Terminal Node Controller.

**TC** Telecommand.

**TDD** Time-Division Duplex.

**TLE** Two-Line Element set.

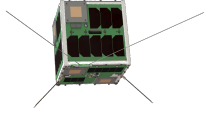
**TM** Telemetry.

**TUBSAT** TU Berlin Satellite.

**UTC** Coordinated Universal Time.

**UTNC** UHF Terminal Node Controller.

## Abstract



This is a living Work In Progress (WIP) document to describe the TUBiX10 modulation, encoding and frame format, currently used in the S Band Network for Cooperative Nanosatellites (S-Net)[1] and the Spectrum Analysis Satellite (SALSAT)[2], both a TU Berlin Satellite (TUBSAT). TUBiX10 is a cube-shaped satellite bus with an edge length of 240 mm and a mass of approximately 10 kg – it's not following the CubeSat standard. The mission objectives are Amateur related, combined with educational and scientific purposes. For further information please refer to the project websites. The document leads through all needed layers of demodulation, decoding and data interpretation, giving two examples for receiving standard telemetry.

## 1 Tracking

To “find” a satellite the most common way is the usage of a Two-Line Element set (TLE) for this specific space object. These objects are organized by globally unique identifiers like the Satellite Catalog Number (SCN) number or Committee on Space Research (COSPAR) catalog ID, independent from their satellite or mission names. Because the UHF links are located in the Amateur Radio band a callsign is needed by which the radio signal can be easily identified. The TUBiX10 satellites are listed in the most common databases from Space Track, CelesTrak, AMSAT, SatNOGS etc. The TUBiX10 IDs and callsigns are collected in table 1.

Satellite	TU Berlin	SCN	COSPAR ID	Callsign
S-Net A	TUBSAT-13	43188	2018-014J	DP0TB
S-Net B	TUBSAT-14	43187	2018-014H	DP0TB
S-Net C	TUBSAT-15	43189	2018-014K	DP0TB
S-Net D	TUBSAT-16	43186	2018-014G	DP0TB
SALSAT	TUBSAT-22	46495	2020-068K	DP0TB

Table 1: Tracking information

**SALSAT LEOP** A special case is the Launch and Early Orbit phase (LEOP). Space monitoring systems like the North American Aerospace Defense Command (NORAD) need some days to identify new space objects. Therefore launch providers are giving state vectors at the moment of satellite separation to their clients. These vectors can be converted to TLEs knowing some basic parameters of the satellite. For SALSAT the flight dynamics model predicted the preliminary TLE shown in listing 1.

```
SALSAT LEOP
1 99826U 20001a 20272.61541667 .00000000 00000-0 -97931-4 0 00014
2 99826 097.6633 206.2144 0014380 237.8618 135.4552 15.02431342000011
```

Listing 1: SALSAT LEOP TLE

There are lots of manuals how to import this text data into orbit prediction tools like Gpredict. Always keep in mind that the predicted orbit is just a rough estimate until it's tracked by a radar system. As of the publishing date of this document the current launch and commissioning timeline is scheduled for **2020-09-28**:

- 11:20:32 UTC Launch
- 14:46:12 UTC Separation
- 23:11:37 UTC First contact

## 2 Frequency

As for all TUBSATs the UHF center frequency is 435.950 MHz for both, the up- and downlink direction. The satellites are transmitting and receiving on this fixed frequency, hence the Doppler shift must be corrected by the ground stations.

## 3 Modulation

TUBiX10 satellites are using a CMX469 FFSK modem chip (see appendix B) and a TCM3 FM transceiver for UHF communications. This chip can generate 1k2, 2k4 or 4k8 Baud FSK signals, ready to be sent to an FM modulator. For a reliable connection TUBiX10 satellites are transceiving via a 1k2 configuration, which uses tones at 1200 and 1800 Hz – with the lower tone representing the bit value 1 and the higher tone representing 0. Note that the tone frequencies are different from the tones at 1200 and 2400 Hz of the Bell 202 modem, used in 1k2 AFSK packet radio!



Figure 1: CMX469 Modem

## 4 Channelization

The UHF communication is handled on the same frequency channel using Time-Division Duplex (TDD). Furthermore Go-Back-N Automatic Repeat Request (ARQ) at the level of the following packet layer (see *LTU Header* in section 5) can be used. The receiving station responds only one time, the transmitting station waits for an answer and repeats the message if no Frame Synchronization Marker (FrSync) was found. So the packets can only collide for one time. This semiduplex ping-pong mechanism is not synchronized in time on the symbol level. Accordingly, there is no constant TDD frame interval of these two forward and return packet types – each participant answers immediately. Both satellite and ground station are sending always one packet at a time, while both directions can have different symbol rates or coding schemes.

## 5 Frame Structure

A TUBiX10 packet transmitted over radio is called Air/Radio Interface (AIR) frame (see figure 2) which consists basically of a Link Transmission Unit (LTU) preamble and header as well as a Payload Data Unit (PDU) header followed by the data itself. For a radio transmission the LTU parts are mandatory. Sent without any data the AIR frame will become a simple beacon signal. The LTU frame header is always coded with block code ( $r = 0.5$ ) and has the maximum possible SNR for the active symbol rate.

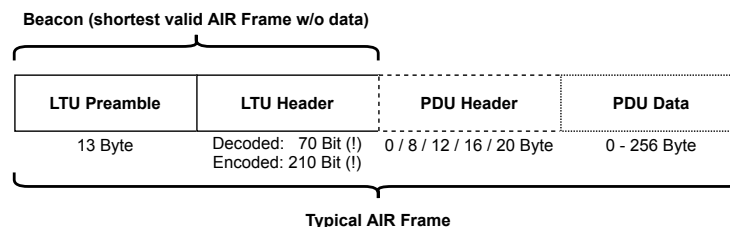


Figure 2: Air/Radio Interface Frame

### 5.1 Link Transmission Unit (LTU)

See S-Net reference document [3] section 2.4 for the specifications of the LTU preamble and header.

## 5.2 Payload Data Unit (PDU)

Figure 3 depicts the general structure of a TUBiX10 PDU. The current TUBiX10 communication protocol which is used for SALSAT extends the first generation S-Net frame header. Therefore a valid TUBiX10 standard PDU header is 8 or 12 Bytes long, because the **Time Tag** is optional using this basic frame format. If the **Extended** flag (formerly called *Future Use*) is set, the PDU header becomes an extended header which is 8 Bytes longer. SALSAT uses this header type by default.

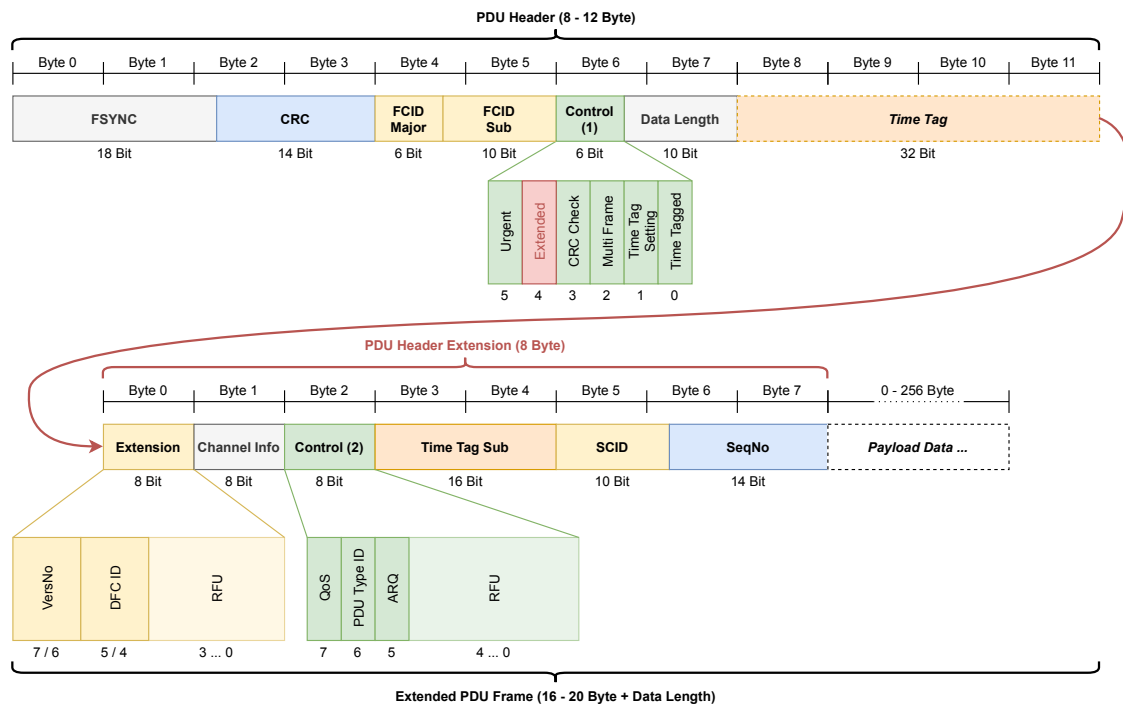


Figure 3: Payload Data Unit

### 5.2.1 PDU Header

The basic header consists of 12 Bytes for frame synchronization (FSYNC), error checking using a CRC checksum, specification of the frame content called FCID Major/Sub, a Control (1) flag register and the Data Length of the packet. Attaching a 4 Byte Time Tag is optional.

**FSYNC** The frame synchronization pattern is predefined with 0b111100110101000000.

**CRC** A 14-bit Cyclic Redundancy Check (CRC) is used for error checking. The so-called CRC-14 is obtained by starting from Byte 4 (FCID Major) until the end of the payload data. 0x21E8 creates the generator polynomial. The initial value starts with 1, 0x3FFF respectively.

**FCID Major** The Frame Content ID Major defines the component context the packet belongs to or is assigned to a specific purpose. For example the Major ID #0 declares a packet related to the Attitude Determination and Control System (ADCS) housekeeping while the ID #9 stands for the Electric Power System (EPS) housekeeping. Since the Major IDs are coded within 6 bits,

there are only 64 possibilities where almost all of them were already assigned to S-Net components. Therefore specific discontinuities are used to address SALSAT payloads. Table 2 shows all currently used FCID Major ranges.

Major ID	Acronym	Component/Purpose
0 - 2	ADCS	Attitude Determination and Control System
3 - 6	PAYLOAD	Payload (SALSAT ff.)
7 - 8	ADCS DBG	Attitude Determination and Control System, Lab Debugging
9 - 11	EPS	Electric Power System
17 - 19	SAT	On-Board Computer (OBC)
25 - 27	HK	Housekeeping Telemetry
32 - 35	FDIR	Failure Detection Interrupt Routine Reports
36 - 37	PAYLOAD DBG	Payload, Lab Debugging (SALSAT ff.)
38 - 39	FDIR DBG	Failure Detection Interrupt Routine Reports, Lab Debugging
40 - 42	LINK	Communication Link (Space Segment)
47 - 50	PDH/STNC	Payload Data Handling
51 - 53	RW	Reaction Wheels
54 - 56	COM	Communication System
57 - 58	LINKGS	Communication Link (Ground Segment)
59 - 60	EGSE	Electrical Ground Support Equipment

Table 2: FCID Major Listing

**FCID Sub** With the Frame Content ID Sub a specific Telemetry (TM) or Telecommand (TC) set of a particular subsystem is defined which allows parsers to interpret the payload data. The most common FCID Sub is #0 indicating a standard TM for every major component (see FCID Major). Table 3 shows the FCID Sub ranges for SALSAT payload subsystems.

Sub ID	Acronym	Subsystem
0 - 199	PDH/PLEPS	Payload Data Handling / PayLoad EPS
200 - 399	SALSA	Spectrum Analysis of LEO Satellite Allocations
400 - 599	FDA	Fluiddynamic Actuator
600 - 799	IPU	Image Processing Unit
800 - 1024	RFU	Reserved for Future Use

Table 3: FCID Sub Listing (SALSAT Payloads)

**Urgent** Flag for the priority of a packet:

- 0 Normal
- 1 Urgent

**Extended** Flag to switch between standard/basic and an extended frame including a PDU header extension:

- 0 Standard Frame (S-Net)
- 1 Extended Frame (SALSAT ff.)

**CRC Check** Flag for CRC usage:

- 0 Ignore CRC
- 1 Generate/Check

**Multi Frame** Flag to control the further processing of the frame:

- 0 Single Frame
- 1 Multi Frame (fragmented payload)

**Time Tag Setting** Flag to declare the type of a timestamp:

- 0 Relative Timestamp
- 1 Absolute Timestamp

**Time Tagged** Flag to indicate the presence of a timestamp:

- 0 Instant Processing
- 1 Time Tagged

**Data Length** Payload data size in Bytes. A Single Frame can hold up to 256 Bytes payload, a Multi Frame up to 1072 Bytes.

**Time Tag** This field is optional and switched by the Control (1) flag **Time Tagged**. Attention: The value is transmitted with the Least Significant Bit (LSB) first! An absolute timestamp represents the Coordinated Universal Time (UTC) in 0.5 seconds since 2000-01-01 00:00:00. The on-board software generates standard TM for all (sub)systems each 500 ms. The timestamp corresponds to the moment of generation. A relative timestamp represents the passage of time after a successfully parsed frame in a resolution of 0.5 seconds.

### 5.2.2 PDU Header Extension

For the more complex SALSAT on-board communication system an extension of the TUBiX10 frame was needed, requiring a backward compatibility to the S-Net communication system. This section begins with an **Extension** subheader containing the specifications related to parsing the header and handling the data payload. It furthermore consists of the **Channel Info**, a **Control (2)** flag register of an extended frame, **Time Tag Sub** for more accurate timing, a Spacecraft ID ( **SCID** ) and a Sequence Number ( **SeqNo** ).

**VersNo, Extension** The Version Number of the extended header is a 2-bit field beginning with zero for SALSAT. As a side note: S-Net satellites don't use extended frames and therefore are not versioned.

VersNo	Satellites
0b00	SALSAT
0b01	–
0b10	–
0b11	–

Table 4: Satellites using a specific protocol version

**DFC ID, Extension** The Data Field Construction Identifier allows to specify the content of the data field to be not only generic data but for instance additional encoded frames. As of protocol version 0 (SALSAT) this field isn't used and statically set to 0b11.

**RFU, Extension** Reserved for Future Use.

**Channel Info** This field contains the source and destination information of an extended frame. It defines the communication path between components like On Board Computer (OBC), UHF Terminal Node Controller (UTNC), S band Terminal Node Controller (STNC) etc. within the satellite bus – AIR declares communication to other external components. If the devices aren't connected directly, the channel ID doesn't matter and is irrelevant for sending or receiving TUBiX10 data. Therefore this field is described in appendix A as an additional information.

**QoS, Control (2)** Quality of Service flag, which is currently not handled:

- 0 Sequence controlled service
- 1 Expedited service

**PDU Type ID, Control (2)** Payload Data Unit type definition:

- 0 Service Data Unit (SDU)
- 1 Supervisory Protocol Data Unit (SPDU) which is some kind of service packet to keep up or configure communication, see also CCSDS Proximity-1 documentation

**ARQ, Control (2)** Flag for ARQ usage, see also **SeqNo** :

- 0 No ARQ
- 1 ARQ

**RFU, Control (2)** Reserved for Future Use (flag fields).

**Time Tag Sub** Time in milliseconds beginning from the last absolute **Time Tag** . This allows subsystems to work one minute without an absolute time. If that's not possible they can increment the absolute time.

**SCID** The Spacecraft Identifier addresses the satellite.

SCID	Satellite
0	S-Net A
1	S-Net B
2	S-Net C
3	S-Net D
4	SALSAT

Table 5: Spacecraft IDs

**SeqNo** Due to the field size there are 16384 Sequence Numbers – enough for a command list of a single pass. As primary element of the ARQ protocol, missing sequence numbers are repeated. For a simple forward error correction on a broadband channel packets can be repeated – multiple arriving data sets are discarded before forwarding. This number is incremented on each packet transmission of a communication system and restarts at the beginning of every (re-)established session.



## 6 Payload Data Formatting

See S-Net reference document [3] section 3.1.3 for specifications regarding the payload data handling.

## 7 Telemetry Definitions

See S-Net reference document [3] section 4 for the specifications of standard telemetry.

## 8 Software Decoder

Instead of the complex handling of hardware MODEMs and TNCs, Software-defined radio (SDR) technology allows the signal processing using common computer architectures. The Satellite Networked Open Ground Station (SatNOGS) extends this concept to the idea of building a distributed global ground station network. Based on the *gr-satellites* decoder [4] there are currently two merge requests [5] [6] pending to integrate the direct reception of TUBiX10 satellites into SatNOGS.

## References

- [1] Chair of Space Technology, S-Net [https://www.space.tu-berlin.de/menue/research/current\\_projects/s\\_net/](https://www.space.tu-berlin.de/menue/research/current_projects/s_net/)
- [2] Chair of Space Technology, SALSAT [https://www.space.tu-berlin.de/menue/research/current\\_projects/salsat/](https://www.space.tu-berlin.de/menue/research/current_projects/salsat/)
- [3] TUBiX10 Telemetry Frames [https://www.raumfahrttechnik.tu-berlin.de/fileadmin/fg169/amateur-radio/TUBIX10\\_3800\\_TN03\\_TM\\_Frame\\_01.pdf](https://www.raumfahrttechnik.tu-berlin.de/fileadmin/fg169/amateur-radio/TUBIX10_3800_TN03_TM_Frame_01.pdf)
- [4] GNU Radio decoders for several Amateur satellites: <https://github.com/daniestevez/gr-satellites>
- [5] Merge Request: SNet Flowgraph for gr-satnogs [https://gitlab.com/librespacefoundation/satnogs/gr-satnogs/-/merge\\_requests/214](https://gitlab.com/librespacefoundation/satnogs/gr-satnogs/-/merge_requests/214)
- [6] Merge Request: Fixes for SALSAT [https://gitlab.com/librespacefoundation/satnogs/gr-satnogs/-/merge\\_requests/215](https://gitlab.com/librespacefoundation/satnogs/gr-satnogs/-/merge_requests/215)

## A Channel Info

The channel ID is important for point-to-multipoint and multipoint-to-multipoint communication interfaces, where a direct addressing of the target device is not possible. For example if the OBC needs to send data to UTNC0 (COM0) it broadcasts the message on the serial interface. If STNC0 is powered and active both TNCs will get the same message and – without further information available in the frame header – transfer this message on their AIR interfaces (UHF and S band). The ground station would receive the same message twice in this case. To prevent this a dedicated channel ID is used at some places. Important cases:

1. For the case the OBC received a message from an external device, e.g. from one of the reaction wheels or from PDH, or from FDA and this message needs to be transmitted to UTNC0 the channel ID needs to be changed to 'OBC0 TO TNC0' or 'OBC1 TO TNC0', the CRC of the message needs to be re-calculated. Now the message can be transmitted to TNC0. If the channel ID differs from 'OBC0 TO TNC0' and from 'OBC1 TO TNC0' the message is not going to be transmitted to the ground station.
2. The long time telemetries from the flash storage, called historic TMs: After reading from the memory the channel IDs need to be adapted too (see above).
3. If (for SALSAT) there is no difference between OBC0 and OBC1 in the code, both OBC0 or OBC1 channel IDs can be used. I.e. there is no difference if the UTNC0 receives a message with 'OBC0 TO TNC0' or with 'OBC1 TO TNC0'. Both messages will be transferred on the AIR interface to ground.
4. In special cases the channel IDs (SALSAT specific) from the list below can be used. E.g. for SALSA(source)→PDH(sink) and for SALSA(source)→PDH(intermediate)→OBC(sink) communication.

For point-to-point communication (e.g. OBC↔PDH or PDH↔SALSA etc.) the channel info is not required and can be set to 'INT0' (Channel 0) or without changes (in case of a message forwarding). On these point-to-point interfaces the channel ID is optional and can be set to zero:

- OBC ↔ PDH PLEPS (SALSA PDH)
- PDH ↔ SALSA
- PDH ↔ SLink
- PDH ↔ IPU
- FDA ↔ PDH
- IPU ↔ CAM
- STNC ↔ IPU

On these interfaces a valid channel ID is required:

- OBC ↔ UTNC
- OBC ↔ STNC
- UTNC ↔ ground
- STNC ↔ ground

On these point-to-point interfaces the channel ID is optional but defined:

- UTNC ↔ ground
- STNC ↔ ground

Source	Destination	Channel	Source	Destination	Channel
UTNC0	OBC	0	OBC0	UTNC0	132
UTNC1	OBC	1	OBC0	UTNC1	133
STNC0	OBC	2	OBC0	STNC0	134
STNC1	OBC	3	OBC0	STNC1	135
UTNC0	AIR	128	OBC1	UTNC0	136
UTNC1	AIR	129	OBC1	UTNC1	137
STNC0	AIR	130	OBC1	STNC0	138
STNC1	AIR	131	OBC1	STNC1	139

Table 6: Channel Info (Space Segment)

Source	Destination	Channel	Source	Destination	Channel
PDH	OBC	4	SALSA	OBC	28
PDH	SALSA	5	SALSA	PDH	29
PDH	SLink	6	SALSA	SLink	30
PDH	CAM	7	SALSA	IPU	31
OBC0	IPU	8	IPU	OBC	32
OBC0	SALSA	9	IPU	SALSA	33
OBC0	PDH	10	IPU	SLink	34
OBC0	FDA0	11	IPU	CAM	35
OBC0	FDA1	12	IPU	FDA0	36
OBC0	FDA2	13	IPU	FDA1	37
OBC0	RW0	14	IPU	FDA2	38
OBC0	RW1	15	IPU	RW0	39
OBC0	RW2	16	IPU	RW1	40
OBC0	CAM	17	IPU	RW2	41
OBC1	IPU	18	FDA0	OBC	42
OBC1	SALSA	19	FDA0	PDH	43
OBC1	PDH	20	FDA0	IPU	44
OBC1	FDA0	21	FDA1	OBC	45
OBC1	FDA1	22	FDA1	PDH	46
OBC1	FDA2	23	FDA1	IPU	47
OBC1	RW0	24	FDA2	OBC	48
OBC1	RW1	25	FDA2	PDH	49
OBC1	RW2	26	FDA2	IPU	50
OBC1	CAM	27			

Table 7: Channel Info (SALSAT specific)

Source	Destination	Channel	Source	Destination	Channel
GS SLink	Server	126	PDH	GS	140
GS UHF	Server	127	SALSA	GS	141
GS SLink	AIR	149	IPU	GS	142
GS UHF	AIR	150	FDA	GS	143
Server	GS SLink	151	RW	GS	144
Server	GS UHF	152			

Table 8: Channel Info (Ground Segment)



## B CMX469 Datasheet

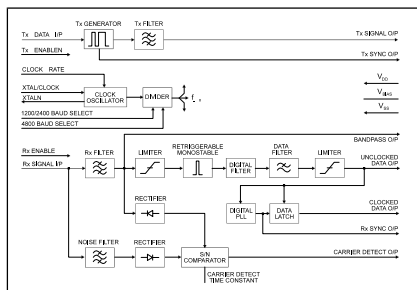
D/469A/3 June 2009

## Features

- Full-Duplex FFSK/MSK Modem with Separate Rx and Tx Enable Functions
- Pin Selectable Data Rates:  
1200, 2400 or 4800 Baud
- Pin Selectable Xtal/Clock Inputs:  
1.008MHz or 4.032MHz
- Clock Recovery Facility
- Carrier Detect Facility
- Low Power Operation (2.0mA typ. at 3.0V)

## Applications

- Data-Over Radio
- Personal/Cordless Telephone
- Radio and General Applications
- Narrowband Coax Data Channels
- Two Way Radio (MPT1327) Signalling
- Portable Data Terminals



## 1.1 Brief Description

The CMX469A is a single-chip CMOS LSI circuit which operates as a full-duplex 1200, 2400 or 4800 baud FFSK/MSK modem. The mark and space frequencies are 1200/1800, 2400/2400 and 2400/4800 Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point. A common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) provides baud-rate, transmit frequencies, and Rx and Tx synchronization.

The transmitter and receiver operate entirely independently, including the individual section powersave functions. The CMX469A includes on-chip circuitry for Carrier Detect and Rx Clock recovery, both of which are made available as output pins. Rx, Tx and Carrier Detect paths contain bandpass filters to optimise signal conditions in each section of the modem. The CMX469A demonstrates good sensitivity and bit-error-rate under adverse signal conditions. The Carrier Detect time constant is set by an external capacitor, so that the product's performance can be optimised in high noise environments. This low-power device operates from a single supply between 2.7V and 5.5V, requires few external components and is available in a wide variety of plastic packages.

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## 1.2 Block Diagram

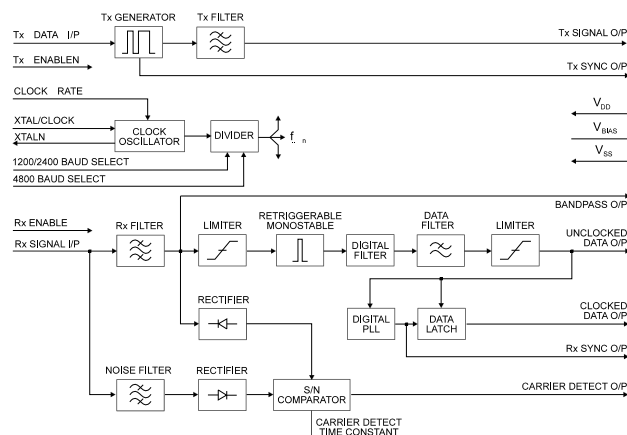


Figure 1 Block Diagram

## 1.3 Signal List

CMX469A		Signal		Description
D3	E2	Name	Type	
Pin No.	Pin No.			
1	1	CLOCK/XTAL	I/P	The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or an external clock. Clock frequency selection is by means of the CLOCK RATE pin. This affects the operational data rate of the device. Operation of any CML microcircuit without a Xtal or clock input may cause device damage.
2	2	XTALN	O/P	The output of the on-chip inverter.
3	3	Tx SYNC O/P	O/P	A squarewave, produced on-chip, to synchronize the input of logic data and transmission of the FFSK/MSK signal.
4	5	Tx SIGNAL O/P	O/P	When the transmitter is enabled, this pin outputs the FFSK/MSK signal. With the transmitter disabled, this pin is set to a high-impedance state.
5	7	Tx DATA I/P	I/P	The serial logic data to be transmitted is input to this pin.
6	8	Tx ENABLE	I/P	A logic '0' will enable the transmitter. A logic '1' at this input will put the transmitter into powersave whilst forcing Tx SYNC OUTPUT to a logic '1' and Tx SIGNAL OUTPUT to a high-impedance state. This pin is internally pulled to V <sub>DD</sub> .
7	9	BANDPASS O/P	O/P	The output of the Rx Bandpass Filter. This output impedance is typically 10kΩ and may require buffering prior to use.
8	10	Rx ENABLE	I/P	The control of the Rx function
9	11	V <sub>BIAS</sub>	BI	The output of the on-chip analogue bias circuitry. Held internally at V <sub>DD</sub> /2, this pin should be decoupled to V <sub>SS</sub> by a capacitor (C2). This bias voltage is maintained under all powersave conditions.
10	12	V <sub>SS</sub>	PWR	Negative supply rail (GND).
11	13	UNCLOCKED DATA O/P	O/P	The recovered asynchronous serial data output from the receiver.
12	14	CLOCKED DATA O/P	O/P	The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the Rx SYNC O/P.

CMX469A		Signal		Description
D3	E2			
Pin No.	Pin No.	Name	Type	
13	15	CARRIER DETECT O/P	O/P	When an FFSK/MSK signal is being received this output is a logic '1'.
14	16	Rx SIGNAL I/P	I/P	The FFSK/MSK signal input for the receiver. This input should be coupled via a capacitor, C3.
15	18	Rx SYNC O/P	O/P	A flywheel squarewave output. This clock will synchronize to incoming Rx FFSK/MSK data.
16	19	1200/2400 BAUD SELECT	I/P	A logic '1' on this pin selects the 1200 baud option. Tone frequencies are: one cycle of 1200Hz represents a logic '1', one-and-a-half cycles of 1800Hz represents a logic '0'. A logic '0' on this pin selects the 2400 baud option. Tone frequencies are: one-half cycle of 1200Hz represents a logic '1', one cycle of 2400Hz represents a logic '0'. This function is also used, in part, to select the 4800 baud option. This pin has an internal 1M $\Omega$ pullup resistor.
17	20	4800 BAUD SELECT	I/P	A logic '1' on this pin combined with a logic '0' on the 1200/2400 BAUD SELECT pin will select the 4800 baud option (1M $\Omega$ pulldown resistor). Tone frequencies are: one-half cycle of 2400Hz represents a logic '1', one cycle of 4800Hz represents a logic '0'. Operation at 4800 baud is only achieved by using a 4.032MHz Xtal or clock.
18	21	CLOCK RATE	I/P	A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
19	22	CARRIER DETECT TIME CONSTANT	BI	Part of the carrier detect integration function. The value of C4 connected to this pin will affect the carrier detect response time and hence noise performance.
20	24	V <sub>DD</sub>	PWR	Positive supply rail. A single 2.7 to 5.0 volt supply is required. This pin should be decoupled to V <sub>SS</sub> by a capacitor (C5). No internal connection, do not use.

Notes: I/P = Input O/P = Output BI = Bidirectional PWR = Power

### 1.5 General Description

The CMX469A has two sections, apart from the Xtal oscillator circuit and clock dividers. These sections may be independently powersaved.

#### Transmitter

The transmitter is enabled by taking Tx EnableN low. Serial data applied to Tx Data Input is sampled internally and an FFSK/MSK sequence is generated. After filtering, this is output at Tx Signal O/P and the transmit clock derived from this signal is output at Tx Sync O/P.

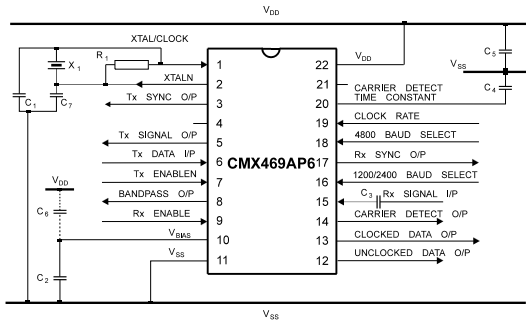
#### Receiver

The receiver is enabled by taking Rx Enable high. The signal applied to Rx Signal I/P is filtered and recovered as serial data from the Unclocked Data O/P. A flywheel synchroniser is used to extract a clock from the recovered serial data stream. The clock is available at Rx Sync O/P and the retimed serial data is available at Clocked Data O/P.

The integrated peak values of the Rx amplitude are compared with out-of-band noise levels and used to make a signal-to-noise assessment, which is available at Carrier Detect O/P.

A Bandpass O/P is also available from the output of the first Rx filter stage, but will require buffering before use.

### 1.4 External Components



Component	Value
R1	1.0M $\Omega$
C1	33.0pF
C2	1.0 $\mu$ F
C3	0.1 $\mu$ F
C4	0.1 $\mu$ F
C5	1.0 $\mu$ F
C6	1.0 $\mu$ F
C7	33.0pF
X1	1.008MHz or 4.032MHz

#### Notes:

- V<sub>BIAS</sub> may be decoupled to V<sub>SS</sub> and V<sub>DD</sub> using C2 and C6 when input signals are referenced to the V<sub>BIAS</sub> pin. For input signals referenced to V<sub>SS</sub>, decouple V<sub>BIAS</sub> to V<sub>SS</sub> using C2 only.
- The performance of the Carrier Detect function will be affected by the nature of the noise spectrum in the received channel. The value of C4 determines the Carrier Detect Time Constant. A long time constant results in improved noise immunity but increased response time. C4 may be varied to trade-off response time for noise immunity.
- A 4.032MHz Xtal/clock is required for 4800 Baud operation.

Figure 2 Recommended External Components

### 1.6 Application Notes

#### 1.6.1 Rx Enable

The control of the relevant outputs with reference to the Rx Enable input is described below:

Rx Enable	Rx Function	Clock Data O/P	Carrier Detect O/P	Rx Sync Out
'1'	Enabled	Enabled	Enabled	Enabled
'0'	Powersave	'0'	'1' or '0'	'1' or '0'

After enabling the Receiver, a time of at least 8 bit periods plus 2ms should be allowed for the Carrier Detect circuit to stabilise and give a valid output.

#### 1.6.2 Operational Data Rate Configurations

Operational Data Rate Configurations are as described below:

Xtal/Clock Frequency	1.008MHz			4.032MHz		
Clock Rate	'0'		'0'	'1'	'1'	'1'
1200/2400 Select	'1'		'0'	'1'	'0'	'0'
4800 Select	'0'		'0'	'0'	'0'	'1'
Baud Rate	1200		2400	1200	2400	4800

#### 1.6.3 Test Set Up

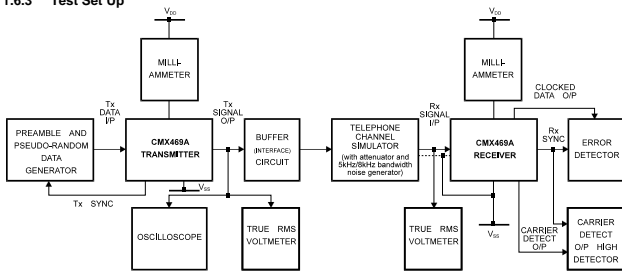


Figure 3 Suggested CMX469A Test Set-Up

### 1.6.4 Synchronous Modem Design Considerations

The CMX469A is an easily applied data pump which can be used with many protocols. Because it is an MSK (minimum shift keying) modem, it achieves a more noise resistant, higher data rate in a narrower bandwidth than other FSK (frequency shift keying) modems. This characteristic is especially important for wireless applications because it fundamentally determines the bandwidth of RF transmissions, which are strictly limited and controlled by regulatory agencies. Using MSK signalling, the CMX469A data modem can achieve a 2400 bps data rate within the typical 300-3000 Hz voice band of many common radios.

In order to achieve this advantage, an MSK modem must precisely control the bit rate and timing of the modulated Tx output signal bits. This control is asserted by the MSK modem with a data clock signal which is output by the modem to pace the Tx data source (e.g. a microcontroller). The data clock signal, in effect, indicates when the Tx data source should provide the next Tx data bit to the modem. See Figure 4. Because this type of interface involves the use of a modem-generated bit clock signal to control the timing of when new Tx data bits must be supplied from the data source, the interface is called synchronous.

Another characteristic of a synchronous modem is that, to receive data, it must first learn the data bit timing of the Rx signal stream before it can accurately demodulate Rx data bits. Accordingly, a synchronous modem undergoes a period of training or synchronisation when it first begins to receive a stream of MSK-modulated signal. During this initial receive phase, the received signal is evaluated over several bit times as the modem 'locks-on' and achieves proper receive synchronisation. This training sequence, called a preamble, is a specific data pattern which must be added to the 'front' of a transmit data stream with the start of each new transmission. A specific preamble data pattern (e.g. 16 bits of alternating 0101 .... for the CMX469A) is used to optimise the training accuracy while minimising the number of preamble bits required.

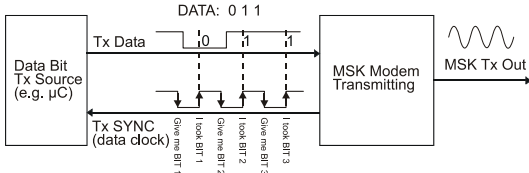


Figure 4 Synchronous Transmit Operation

Non-synchronous or asynchronous interfaces are commonly found in wired applications which do not have the bandwidth efficiency requirements of wireless systems. A well-known example is the serial port of a personal computer, which can transmit a 1200 bps (or faster) data signal without using an additional data clock signal to control the precise rate and timing of data bits being transmitted to a typical telephone line modem. This is achieved by preceding the sequence of data bits with a START bit and terminating the sequence of data bits with a STOP bit. The timing of the Rx signal stream can be determined by examining the duration of the START bit to a sufficient accuracy for the reception of a short (usually 8 or 9 bit) sequence of data bits. Popular modem standards, such as ITU V.23 and Bell 202, use FSK signalling to pass such asynchronous serial port data signals over telephone systems.

Another aspect of asynchronous interfaces and modems is that they can carry data streams which are not at the exact, nominal data rate. For example, a 1200 bps FSK modem will typically operate properly when supplied with transmit data streams of 1194 to 1206 bps.

## 1.7 Performance Specification

### 1.7.1 Electrical Performance

#### Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply ( $V_{DD} - V_{SS}$ )	-0.3	7.0	V
Voltage on any pin to $V_{SS}$	-0.3	$V_{DD} + 0.3$	V
Current into or out of $V_{DD}$ and $V_{SS}$ pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

D3 Package	Min.	Max.	Units
Total Allowable Power Dissipation at $T_{amb} = 25^{\circ}\text{C}$		560	mW
... Derating		5.6	mW/ $^{\circ}\text{C}$
Storage Temperature	-55	+125	$^{\circ}\text{C}$
Operating Temperature	-40	+85	$^{\circ}\text{C}$

E2 Package	Min.	Max.	Units
Total Allowable Power Dissipation at $T_{amb} = 25^{\circ}\text{C}$		1000	mW
... Derating		10.0	mW/ $^{\circ}\text{C}$
Storage Temperature	-55	+125	$^{\circ}\text{C}$
Operating Temperature	-40	+85	$^{\circ}\text{C}$

Because of the differences in synchronous and asynchronous interfaces, they cannot successfully operate if directly connected. In other words, a personal computer's RS232 serial port cannot directly interface to an MSK modem. This is because:

- The asynchronous interface may provide data bits too fast or too slow compared to the precise rate required for MSK signalling (a bit rate, or pacing, incompatibility).
- The timing of each specific data bit presented by an asynchronous interface will not be aligned with the precise bit timing required for MSK signalling (a bit timing incompatibility).

Synchronous and asynchronous interfaces can be successfully interconnected for applications requiring the advantages of both. This typically involves the use of data buffering and retiming circuits to resolve the timing and pacing issues.

#### Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply ( $V_{DD} - V_{SS}$ )		2.7	5.5	V
Operating Temperature		-40	+85	$^{\circ}\text{C}$
Xtal Frequency	1	4.028	4.036	MHz

Note 1: A Xtal frequency of 1.008MHz (1200/2400 baud only) or 4.032MHz is required for correct operation. A frequency tolerance of  $\pm 0.1\%$  is recommended, but ultimately the tolerance selected will depend upon system requirements.

#### Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD} = 2.7\text{V}$  at  $T_{amb} = 25^{\circ}\text{C}$  and  $V_{DD} = 3.0\text{V}$  to  $5.5\text{V}$  at  $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  
Xtal/Clock Frequency = 4.032MHz, Bit Rate = 1200 baud, Rx Input Level = 300mVrms.

	Notes	Min.	Typ.	Max.	Units
<b>Static Values</b>					
$I_{DD}$ Rx Enabled, Tx Disabled ( $V_{DD} = 5.0\text{V}$ )	2	-	3.6	-	mA
$I_{DD}$ Rx and Tx Enabled ( $V_{DD} = 5.0\text{V}$ )	2	-	4.5	-	mA
$I_{DD}$ Rx and Tx Disabled ( $V_{DD} = 5.0\text{V}$ )	2	-	650	-	$\mu\text{A}$
$I_{DD}$ Rx Enabled, Tx Disabled ( $V_{DD} = 3.0\text{V}$ )	2	-	1.5	-	mA
$I_{DD}$ Rx and Tx Enabled ( $V_{DD} = 3.0\text{V}$ )	2	-	2.0	-	mA
$I_{DD}$ Rx and Tx Disabled ( $V_{DD} = 3.0\text{V}$ )	2	-	300	-	$\mu\text{A}$
Logic '1' Level	1	70%	-	-	$V_{DD}$
Logic '0' Level	1	-	-	30%	$V_{DD}$
Digital Output Impedance		-	4.0	-	k $\Omega$
Analogue and Digital Input Impedance		100	-	-	k $\Omega$
Tx Output Impedance ( $V_{DD} = 5.0\text{V}$ )		-	0.6	1.0	k $\Omega$
<b>Dynamic Values</b>					
<b>Receiver</b>					
Signal Input Dynamic Range SNR = 50dB	3, 4	100	230	1000	mVrms
Bit Error Rate at SNR = 12dB	4, 5	-	-	-	-
1200 Baud		-	2.5	-	$10^{-4}$
2400 Baud		-	1.5	-	$10^{-3}$
4800 Baud		-	1.5	-	$10^{-3}$
Bit Error Rate at SNR = 20dB	4, 5	-	-	-	-
1200/2400/4800 Baud		-	<1.0	-	$10^{-8}$
Receiver Synchronization at SNR = 12dB probability of bit 16 being correct	7	-	0.995	-	-

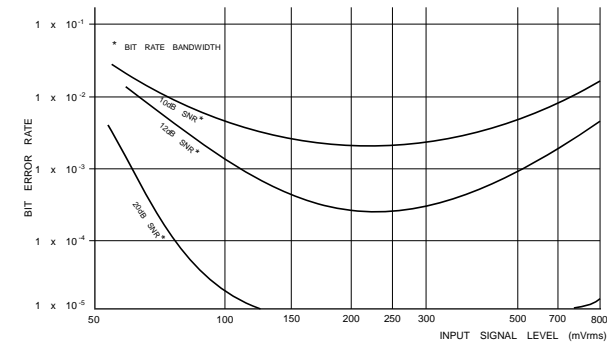
	Notes	Min.	Typ.	Max.	Units
<b>Carrier Detect</b>	3				
Sensitivity	1, 7, 8	-	-	150	mVrms
Probability of CD being High after bit 16: with SNR = 12dB	9		0.995		
with 230mVrms Noise and No Signal	9		0.05		
<b>Transmitter Output</b>					
Tx Output Level	1	-	775	-	mVrms
Output Level Variation for 1200/1800Hz or 1200/2400Hz or 2400/4800Hz		0	-	+/-1.0	dB
Output Distortion	10	-	3.0	5.0	%
3rd Harmonic Distortion	10	-	2.0	3.0	%
<b>Isochronous Distortion</b>					
1200Hz - 1800Hz/1800Hz - 1200Hz		-	25.0	40.0	µs
1200Hz - 2400Hz/2400Hz - 1200Hz		-	20.0	30.0	µs
2400Hz - 4800Hz/4800Hz - 2400Hz		-	10.0	20.0	µs
Logic '1' Carrier Frequency 1200 Baud	6	-	1200	-	Hz
2400 Baud	6	-	1200	-	Hz
4800 Baud	6	-	2400	-	Hz
Logic '0' Carrier Frequency 1200 Baud	6	-	1800	-	Hz
2400 Baud	6	-	2400	-	Hz
4800 Baud	6	-	4800	-	Hz

- Notes:**
1. Measured at  $V_{DD} = 5.0$  volts. Signal levels and thresholds are proportional to  $V_{DD}$ .
  2. Excludes any current drawn by external components, but includes current drawn by the crystal components.
  3. See Figure 7 (Typical Variation of BER with Input Signal Level).
  4. SNR = Signal-to-Noise Ratio in the Bit-Rate Bandwidth.
  5. See Figure 8 (Typical Rx BER vs Signal-to-Noise Ratio).
  6. Dependent upon Xtal tolerance.
  7. With an alternating (1010...) pattern.
  8. Measured with a 150mVrms input signal (no noise).
  9. A signal level of 230mVrms is used in C.D. probability measurements. Noise bandwidth is 5kHz (1200/2400 baud operation) or 8kHz (4800 baud operation). See Section 1.4, Note 2 for details on optimising noise immunity.
  10. For an unmodulated carrier.

**1.7.1 Electrical Performance (continued)**

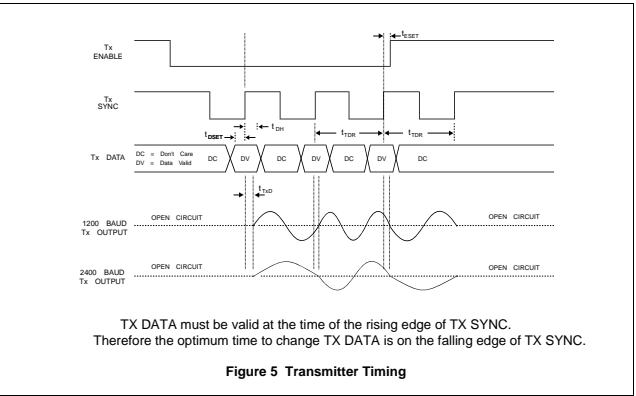
	Interface Timings	Notes	Min.	Typ.	Max.	Units
$t_{ESET}$	Tx Delay, Signal to Disable Time	2	2.0	-	800	µs
$t_{DSET}$	Data Set-Up Time	1	2.0	-	-	µs
$t_{DH}$	Data Hold Time		2.0	-	-	µs
$t_{TXD}$	Tx Delay to O/P Time		-	1.2	-	µs
$t_{TDR}$	Tx Data Rate Period		-	833	-	µs
$t_{RDR}$	Rx Data Rate Period	2	800	-	865	µs
	Undetermined State (see Figure 6)		-	-	2.0	µs
$t_{ID}$	Internal Rx Delay		-	1.5	-	ms

- Notes:**
1. Consider the Xtal/Clock tolerance.
  2. 1200 Baud example.

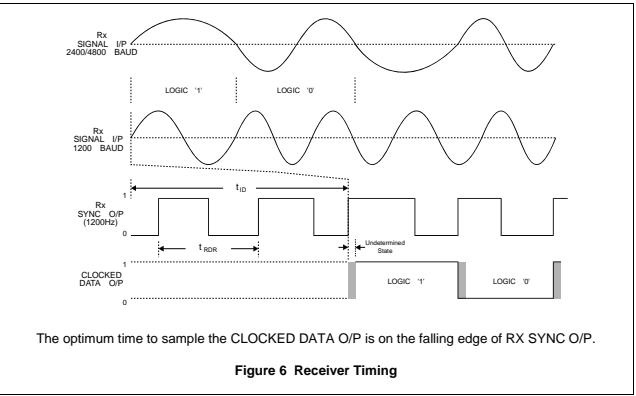


**Figure 7 Typical Variation of Bit Error Rate with Input Level**

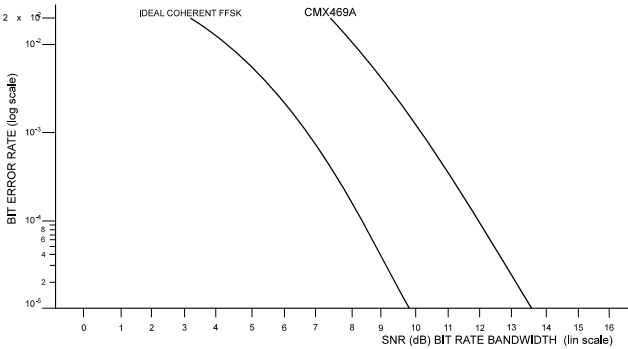
**Interface Timing Diagrams**



**Figure 5 Transmitter Timing**



**Figure 6 Receiver Timing**



**Figure 8 Typical Rx Bit Error Rate vs Signal-to-Noise Ratio**