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FG Mixed Signal Circuit Design

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Master Thesis:

Design of a Ring-Oscillator-based Type-II Charge-Pump Phase-Locked Loop as Reference Generator for a Milli-Meter-Wave Sub-sampling Phase-Locked Loop

In virtual all electronic systems there is a need for periodic signals, either for RF applications like mixers and RADAR or for digital signals (clock). These signals are generated with a phase-locked loop (PLL) controlling an oscillators (via voltage, current, digitally, etc.). The PLL is a negative-feedback system with stability being a major design issue.

The design of high-frequency (milli-meter-wave) PLLs can benefit from a two-stage design where a secondary PLL generates the reference signal for the higher-frequency PLL. This eases the integration of a medium-frequency reference signal and enables advantages of an on-chip implementation like multi-phase outputs.

Two-stage PLL designs usually can allow for relaxed noise requirements of the first PLL, since the out-of-band phase noise is filtered out by the main PLL. Therefore, compact ring-oscillator-based PLLs are feasible, which is desirable for these architectures.

In this work, a type-II charge-pump phase-locked loop with an output frequency of 875 MHz shall be implemented. Some rough circuit implementations already exist, but the overall concept and system design is still to be done. Furthermore, a system analysis for the correct loop response across process corners is necessary.

Goals:

1) Analyze top-level PLL architecture and develop loop filter
2) Implement type-II charge-pump PLL
3) Validate design across process corners

Stretch Goals:

1) Create the layout of the PLL or some subcircuits

Prerequisites:

Bachelor in electrical engineering or comparable, knowledge of integrated analog circuit design (for example MSC courses AIC & AAIC), experience with cadence virtuoso

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