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Elektrotechnik und Informatik

Institut für Technische Informatik
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FG Mixed Signal Circuit Design

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Bachelor/Master Thesis:

Design of a Ring Oscillator with Center Frequency Calibration for improved Stability in Phase-Locked Loops

In virtual all electronic systems there is a need for periodic signals, either for RF applications like mixers and RADAR or for digital signals (clock). These signals are generated with a phase-locked loop (PLL) controlling an oscillators (via voltage, current, digitally, etc.). The PLL is a negative-feedback system with stability being a major design issue.

In analog PLLs, the loop filter establishes the correct frequency response in order to satisfy phase noise requirements and stability. The most crucial parameter is the bandwidth of the PLL, which mainly depends on the main filter capacitor. For proper stability margins, a large capacitor is needed, especially for high frequency oscillators with large gain.

The gain of voltage-controlled oscillators (VCO) is determined by the center frequency of the oscillator, which has to reach the target output frequency of the PLL under the influence of different variations (process, voltage, etc.).

In this work, the implementation of a voltage-controlled ring oscillator with on-chip center frequency calibration shall be analyzed. The main goal of the oscillator is to achieve a matching of the center frequency to the target frequency without the need of a large oscillator gain.

Goals:

1) Design the oscillator at 5 Ghz with minimal frequency gain

Stretch Goals:

1) Check oscillator design in a closed-loop PLL model
2) Create the layout of the oscillator in 22 nm CMOS FDSOI

Prerequisites:

Basic knowledge of analog design and physical implementation (layout) in Cadence Virtuoso, design knowledge of oscillators is a plus

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