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FG Mixed Signal Circuit Design

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Bachelor/Master Thesis:

Implementation of a Transmission-Line Phase Shifter for High Frequency PSK Transmitters

With the advance of modern technologies, high frequency transceivers for wireless communication are increasingly feasible in CMOS processes. The main modulation schemes for data links with high spectral efficiency are quadrature-amplitude modulation (QAM) and amplitude-phase-shift-keying (APSK). While the former is more popular, studies show that the APSK can possibly outperform QAM in terms of noise resistance and efficiency. To achieve amplitude and phase modulation, a phase-locked loop (PLL) with phase control and a variable-gain amplifier can be used. If a regular PLL is to be used, the phase-shifting can be done via a passive phase-shifter, resulting in a more efficient design.

The topic of this thesis is the implementation of a such a phase shifter for phase-based modulation formats such as APSK. There is a working schematic prototype for a transmission-line-based phase shifter, which has to be evaluated in-depth for overall feasability, process variation etc. Furthermore, this work should also focus on the creation of chip-level layout for experimental verification. Additionally, the prototype needs a power amplifier to drive on-chip pads and off-chip measurement equipment.

Goals:

1) Implement a power amplifier as driver for measurement equipment
2) Implement a chip-level layout of the phase-shifter including the power amplifier (LVS-clean and no major design-rule violations)

Stretch Goals:

1) Extend the phase-shifter to support other phase-based modulation formats (QPSK vs. 8-PSK)

Prerequisites:

Basic knowledge of analog design (schematic and layout) in Cadence Virtuoso and basic RF knowledge (matching, characteristic impedance, ...)

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