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Fakultät IV
Elektrotechnik und Informatik

Institut für Technische Informatik
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FG Mixed Signal Circuit Design

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Bachelor/Master Thesis:

High frequency Clock and Data Input Stages

When designing a ADC/DAC based system, the clock and data inputs often are rushed because it is one of the last steps of the design. However, significant performance can be lost with poor design. This is especially true for data inputs, that need broadband termination.

Goals:

1) Analysis of all possibilities of feeding a 50 Ω terminated signal onto the chip
    a. Both for clock signals (high frequency, up to 35 GHz, but low signal bandwidth) as wells as data signals (high baud rate, up to 60 GBaud)
    b. Both single ended and differential
2) Implementing the most promising designs in schematic level
3) Performance comparison

Stretch Goals:

4) Layout and post-layout analysis (mandatory for MA)

Prerequisites:

- Basic knowledge of analog circuit design
- Experience with Cadence Virtuoso (AIC or AAIC knowledge is sufficient)
- Basic knowledge in RF (you should know what S-Parameters are)

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